IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
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ELIYAHOU HARARI et al.)
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Serial No.: 08/789,421)
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Filed: January 29, 1997)
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For: FLASH EEPROM SYSTEM)
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Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend certain of the claims of the above-identified Continued Prosecution

Application, as follows:

1 63. (Twice Amended)   A method of operating a bulk storage memory with a

host processor, wherein the bulk storage memory includes an array of non-volatile floating gate

memory cells, comprising:

storing, within defined non-overlapping groups of array cells, sectors of user data and

associated overhead data, at least some of said overhead data being generated within the bulk storage

memory to include information [either] of at least one of the individual memory array cell groups in

which the overhead data are stored or [of] the user data stored in the same memory array cell groups

as the overhead data,

in response to receipt from the host processor of an address in a format designating

at least one mass memory storage block address, converting said at least one mass memory storage

block address into an address of at least one of the memory array cell groups and addressing said at

least one of the memory array cell groups,